Remarks

I. Introduction

The Office Action rejected claims 1-2, 7-9, 19-20, and 32 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,910,667 to Tanaka et al. (Tanaka). The Office Action rejected claims 3 and 21 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of U.S. Patent No. 5,929,928 to Matsugami et al. (Matsugami). The Office Action rejected claims 3-5, 14-16, and 21-23 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of U.S. Patent No. 5,646,142 to Lavelle et al. (Lavelle). The Office Action rejected claims 6, 17, 24, and 31 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of U.S. Patent No. 6,745,315 to Gurney et al. (Gurney). The Office Action rejected claims 10-13, 18, and 26-27 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of U.S. Patent No. 6,349,380 to Shahidzadeh et al. (Shahidzadeh). The Office Action rejected claims 28-30 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Shahidzadeh, and further in view of Lavelle. The Office Action rejected claims 17 and 31 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Shahidzadeh, and further in view of Gurney.

Claims 1 and 10 have been amended to more particularly point out and distinctly claim the invention.

Claims 1-32 remain for consideration. Applicants believe that claims 1-32 are in condition for allowance.

II. Rejections under 35 U.S.C. §102(b)

Independent claims 1 and 19 were rejected as being anticipated by Tanaka. In order for a claim to be anticipated under 35 U.S.C. §102, **each and every** limitation of the claim must be found either expressly or inherently in a single prior art reference. PIN/NIP, Inc. v. Platte Chem. Co., 304 F.3d 1235, 1243 (Fed. Cir. 2002). In the present case, Tanaka does not show each and

every limitation of independent claims 1 and 19. Therefore, applicants request the withdrawal of the rejections under 35 U.S.C. §102(b).

Claim 1

The present invention is generally directed to a method for concurrently accessing multiple memory locations. As described at page 5, line 10 – page 6, line 7, an index vector contains a plurality of values which are used as indices to access a memory unit. A base value contains the memory address of a first memory location in the memory unit. Each of the values of the index vector is used as an offset from the base value and thus represents a location in the memory unit. In order to identify the memory location that is represented by each of the index vector values, an operation is performed concurrently on each of the index vector values with the base value to generate a plurality of memory addresses. As illustrated in FIGS. 3 and 4, the operation is performed with the same base value for each of the index vector values in order to identify a memory location offset from the memory location specified by the same base value for each of the index vector values. In one embodiment of the present invention, the operation is adding the base value to each of the index vector values. In another embodiment, a bit replacement operation is performed on each of the index vector values with the base value. Each of the plurality of memory addresses is accessed concurrently. For example, the contents of each of the plurality of memory addresses can be retrieved and stored concurrently in a single memory cycle.

Independent claim 1 has been amended to specifically claim the performing an operation on each of the index vector values with the same base value. In particular, amended claim 1 recites, "concurrently performing an operation on individual ones of said plurality of index vector values with a same base value to generate a plurality of memory addresses".

Tanaka does not disclose the limitations of independent claim 1 as amended, and therefore does not anticipate amended claim 1 under 35 USC §102.

Tanaka is generally directed to a vector buffer storage for temporarily storing vector data in a vector processor. The vector processor processes vector data according to instructions. A memory location of vector data in a main storage is given by a start address stored in a vector base register VBR and an increment value stored in a vector increment register VIR. The memory location of the vector data corresponds to a memory location in the main storage that the vector data is loaded from or stored to according to the instructions. As described at column 3 lines 14-16, the VIR holds an increment used to specify one location of vector data in the main memory. As described in Tanaka, numeral 13 of FIG. 1 denotes a group of vector increment registers, each of which hold a single increment values. Numeral 12 of FIG. 1 denotes a group of vector base registers, each of which hold a single base value.

FIG. 3 of Tanaka illustrates two fetch requestors 103 and 104 for fetching vector data stored at two addresses designated by (VB1, VI1) and (VB2, VI2), and a store requestor 105 for storing vector data at an address designated by (VB3, VI3). Each increment value VI1, VI2, and VI3 is paired with a separate start address VB1, VB2, and VB3. The Examiner suggests that the starting values VB1, VB2, and VB3 could be the same value. However, the possibility that the starting values VB1, VB2, and VB3 could be the same is not disclosed anywhere in Tanaka. In fact, FIG. 3 of Tanaka illustrates the memory locations designated by the (VB1, VI1), (VB2, VI2), and (VB3, VI3) in the main storage as three separate tables corresponding to different starting addresses. The Examiner's suggestion that VB1, VB2, and VB3 could be the same value is not sufficient under the strict anticipation standard of 35 U.S.C. §102, without this possibility being disclosed in Tanaka. Therefore, Tanaka fails to disclose "concurrently performing an operation on individual ones of said plurality of index vector values

with a same base value to generate a plurality of memory addresses" as recited in independent claim 1.

Thus, for the reasons discussed above, independent claim 1 is allowable over the cited art. Claims 2-9 are dependent upon an allowable independent claim and are therefore also allowable.

Claim 19

An apparatus for implementing an embodiment of the present invention is illustrated in FIG. 4. As shown in FIG. 4 and described at page 6, line 8 – page 7, line 2, the apparatus includes a an index vector register (402) which stores the index vector and operator circuits (shown as adders 406 in the particular embodiment of FIG. 4), each operator circuit connected to one of the segments of the index vector register. A base value is stored in a register which is connected to each operator circuit. Each segment of the index vector register stores one of the index vector values, and each of the operator circuits concurrently performs the operation with the base value on the index vector value stored in the segment of the index vector register to which it is connected. For example, each adder 406 of FIG. 4 adds the index vector value stores in the segment $i_0 - i_7$ to which it is connected to the base value. In another embodiment of the present invention, operator circuits perform bit replacement on the corresponding index vector values with the base value. As illustrated in FIG. 4, all of the index vector values are stored in a common register and the operator circuits use the same base value to concurrently perform the operation on the index vector values. A memory location is generated corresponding to each of the index vector values, and the memory locations are concurrently accessed.

These aspects of the present invention are recited in independent claim 19. In particular, claim 19 recites an apparatus comprising:

> a first storage register for storing an index vector comprising a plurality of values;

a second storage register for storing a base value;

a plurality of operator circuits, individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on individual ones of said plurality of index vector values with said base value to generate a plurality of memory addresses on outputs of said operator circuits; and

at least one memory unit coupled to the outputs of said operator circuits such that said plurality of memory addresses are accessible in a said at least one memory unit.

Tanaka does not disclose the limitations of independent claim 19, and therefore does not anticipate claim 19 under 35 USC §102.

As described above, FIG. 1 of Tanaka illustrates a group of vector increment registers 13, and each of the vector increment registers holds a single increment value. Accordingly, increment values V1, V2, and V3 of FIG. 3 are each stored in a separate one of the group of vector increment registers. In the Office Action dated October 3, 2006, the Examiner argues that the group of increment values stored in the separate vector increment registers can be considered a vector. However, that the increment values stored in multiple registers could be considered a vector is not the same as a single register storing an index vector comprising a plurality of values. Tanaka does not describe a single storage register storing an index vector having a plurality of values. The Office Action asserts that VI1, VI2, and VI3, 109, 111, and 113 of FIG. 3 and 13 of FIG. 1 show a storage register storing an index vector. However, as described above, reference numeral 13 denotes a group of increment registers each storing a single value, and VI1, VI2, and VI3 are increment values each of which stored in a separate one of the group of increment registers. Reference numerals 109, 111, and 113 refer to the locations designated by VI1, VI2, and VI3 on the main storage, not registers. Thus, Tanaka fails to disclose "a first storage register for storing an index vector comprising a plurality of values" as recited in independent claim 19.

Furthermore, Tanaka does not disclose "a plurality of operator circuits" as recited in claim 19. The Office Actions asserts that the fetch requestors 103 and 104 and the store requestor 105 are illustrative of the claimed "operator circuits". However, FIG. 3 of Tanaka illustrates that each of these requestors inputs a respective one of VI1, VI2, and VI3 and a respective one of VB1, VB2, and VB3. As described at column 3, lines 14-16, each increment value (such as VI1, VI2, and VI3) is stored in a separate vector increment register. Also, each start address (VB1, VB2, and VB3) is stored in a separate base value register. Accordingly, the requestors 103, 104, and 105 are connected to separate increment registers to input VI1, VI2, and VI3. Thus, the requestors 103, 104, and 105 do not each have a first input coupled to a portion of a single storage register storing an index vector. Furthermore, the requestors 103, 104, and 105 are connected to separate base value registers to input VB1, VB2, and VB3. Thus, the requestors 103, 104, and 105 do not each have a second input coupled to a single storage register storing a base value to be used by each requestor 103, 104, and 105. The Examiner suggests that VB1, VB2, and VB3 can be the same value (even though this possibility is not disclosed in Tanaka). Even if VB1, VB2, and VB3 were the same value, they are still stored in separate registers, and the requestors are connected to the separate registers, not a single register storing a base value. Thus, Tanaka fails to disclose "a plurality of operator circuits, individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on individual ones of said plurality of index vector values with said base value to generate a plurality of memory addresses on outputs of said operator circuits," as recited in independent claim 19.

Thus, for the reasons discussed above, independent claim 19 is allowable over the cited art. Claims 20-25 are dependent upon an allowable independent claim and are therefore also allowable.

III. Rejections under 35 U.S.C. §103(a)

Independent claims 10 and 26 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Shahidzadeh. This rejection is traversed for the reasons stated below.

Claim 10

Regarding claim 10, the combined teaching of Tanaka and Shahidzadeh does not result in Applicants' invention as recited in claim 10 and Applicants' invention as recited in claim 10 is not obvious in view of the combined teachings of Tanaka and Shahidzadeh under 35 USC §103.

As described above, Tanaka does not disclose concurrently generating memory addresses using a plurality of values from and index vector with a same base value. Thus, Tanaka fails to disclose "concurrently performing an operation on a value stored in individual ones of said index vector segments with a same base value to generate a first plurality of memory addresses" as recited in independent claim 10 as amended.

In the Office Action, the Examiner admits that Tanaka does not show "adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address," as recited in independent claim 10, but alleges that Shahidzadeh teaches this limitation. The Examiner failed to respond to Applicants' remarks of August 24, 2006 showing that Shahidzadeh does not show this limitation of claim 10.

Shahidzadeh is directed to providing an extended linear address of more than 32 bits. As illustrated in FIG. 9 and described at column 6, lines 7-21 of Shahidzadeh, an extended linear address 916 is generated from a segment register 902 containing a segment selector 904 and a segment extension 914. The segment selector 904 is used to select a descriptor table 906 and a segment descriptor 908 so as provide a base address. An offset value in an offset register 910 is added to the base address to provide a lower portion of the linear address.

The segment extension 914 is concatenated with the lower portion of the linear address to obtain the extended linear address 916. Although Shahidzadeh describes concatenating the segment extension 914 with the lower portion of the linear address, Shahidzadeh does not disclose concatenating a plurality of values in an index vector and adding the base value to the concatenation of the plurality of values of an index vector. As described in Shahidzadeh, the offset is a single value from an offset register 910, not an index vector having a plurality of values. Therefore, Shahidzadeh does not disclose "adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address," as recited in independent claim 10.

Thus, for the reasons discussed above, independent claim 10 is allowable over the cited art. Claims 11-18 are dependent upon an allowable independent claim and are therefore also allowable.

Claim 26

Regarding claim 26, the combined teaching of Tanaka and Shahidzadeh does not result in Applicants' invention as recited in claim 26 and Applicants' invention as recited in claim 26 is not obvious in view of the combined teachings of Tanaka and Shahidzadeh under 35 USC §103.

As described above, Tanaka does not describe a single storage register storing an index vector having a plurality of values. Thus, Tanaka fails to disclose "a first storage register for storing an index vector comprising a plurality of segments" as recited in independent claim 26. Also as described above, Tanaka fails to disclose "a plurality of operator circuits, individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on a value stored in individual ones of said index vector segments with said base value to

generate a first plurality of memory addresses on outputs of said operator circuits," as recited in independent claim 26.

The Examiner failed to respond to Applicants' remarks of August 24, 2006 showing that Shahidzadeh does not show "an adder circuit having a first input coupled to said second storage register and a second input coupled to said first storage register for adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address," as recited in independent claim 26.

Although FIG. 9 of Shahidzadeh illustrates concatenating the segment extension 914 with the lower portion of the linear address, Shahidzadeh does not disclose concatenating a plurality of values in an index vector and adding the base value to the concatenation of the plurality of values of an index vector. As described in Shahidzadeh, the offset is a single value from an offset register 910, not an index vector having a plurality of values. Although the single offset value is added to the base address, Shahidzadeh does not disclose adding a concatenation of a plurality of segments of an index vector to the base. Therefore, Shahidzadeh does not disclose "an adder circuit having a first input coupled to said second storage register and a second input coupled to said first storage register for adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address," as recited in independent claim 26.

Thus, for the reasons discussed above, independent claim 26 is allowable over the cited art. Claims 27-32 are dependent upon an allowable independent claim and are therefore also allowable.

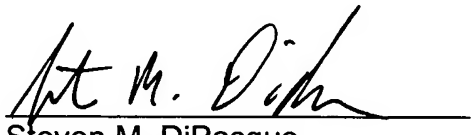
IV. Conclusion

No new matter has been added by the amendments to claims 1 and 10.

Claims 1 and 10, as well as claims 11-18 and 27-32 dependent directly or indirectly thereon, have been amended to present these claims in better from for consideration on appeal, in case the Examiner persists with the rejections of these claims. As such, entry of these amendments is hereby requested pursuant to 37 CFR 1.116(b)(2).

For the reasons discussed above, all pending claims are allowable over the cited art. Reconsideration and allowance of all claims is respectfully requested.

Respectfully submitted,



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